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TITLE: PLL FREQUENCY SYNTHESIZER CIRCUIT

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ABSTRACT:

PURPOSE: To provide a multi-circuit PLL frequency synthesizer circuit without generating the interference of a signal by respective oscillation circuit part and capable of switching a frequency with low power consumption and at high speed.

CONSTITUTION: Standby circuits(STBY) 40, 41 are provided for the VCO 38 of a first PLL frequency synthesizer circuit 52 and the VCO 39 of a second PLL frequency synthesizer circuit 53 in a two-circuit PLL frequency synthesizer circuit 30, respectively, and for example, only the VCO 38 is made to be in an operating state by letting the standby circuit(STBY) 40 be on an operating mode when the PLL frequency synthesizer circuit 52 is used, and by letting the VCO 39 be in a standby state by letting the standby circuit(STBY) 41 of the PLL frequency synthesizer circuit 53 on the other side be on a standby

mode, thereby, the oscillation of the VCO 39 is stopped, and spurious wave can be prevented from occurring. Also, when the frequency is switched, the VCO 39 in the standby state is made to be in the operating state, and the VCO 38 in the operating state is set in the standby state by the standby circuits(STBY) 40, 41.

* NOTICES *

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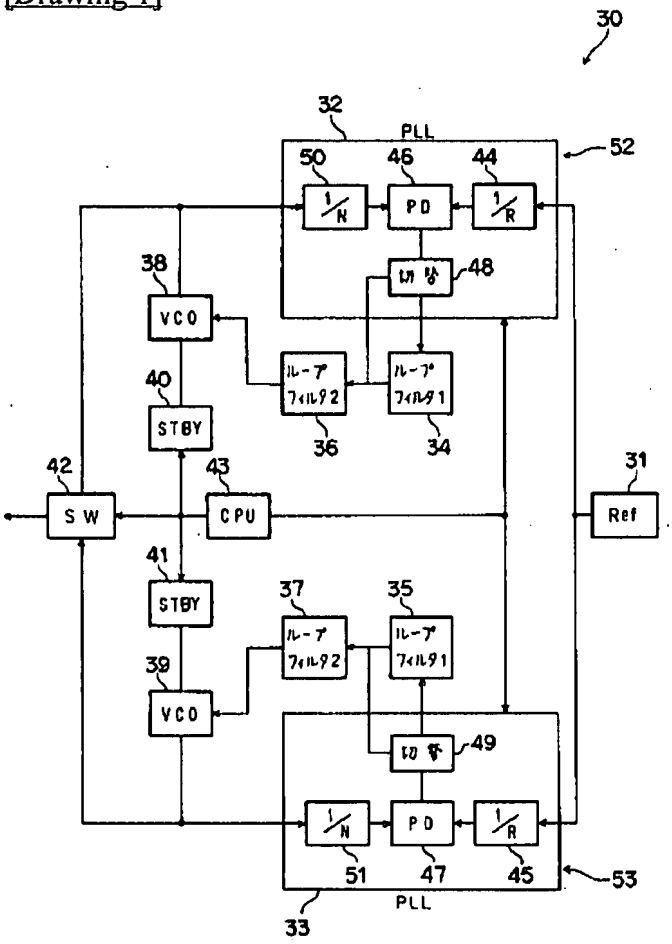
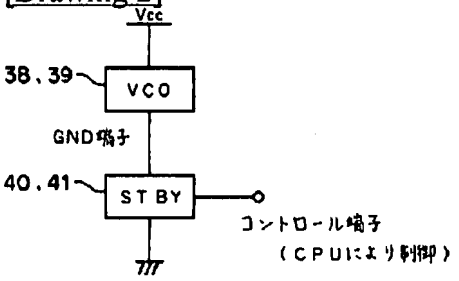
DRAWINGS

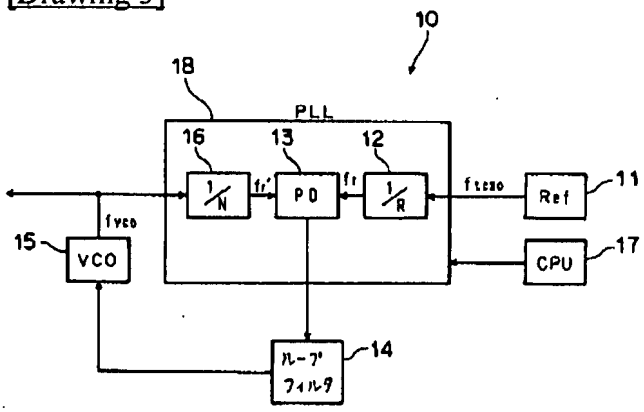
[Drawing 1]



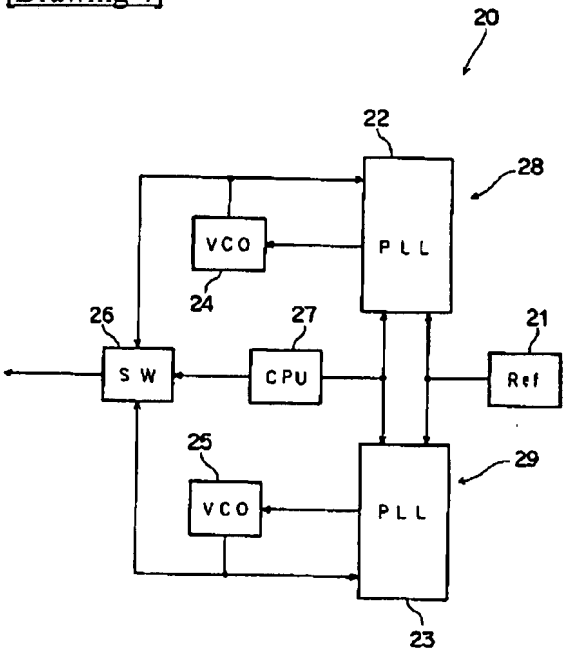
[Drawing 2]



[Drawing 3]



[Drawing 4]



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to a PLL (Phase Locked Loop) frequency synthesizer circuit, and relates to the multi-circuit PLL frequency synthesizer circuit aiming at a high-speed frequency change in detail.
[0002]
[Description of the Prior Art] The PLL frequency synthesizer circuit is used for the tuning circuits of migration band communication equipment, such as a digital cordless telephone and a cellular phone.
[0003] Drawing 3 is the circuitry Fig. of the conventional PLL frequency synthesizer circuit. The PLL frequency synthesizer circuit 10 is constituted by the reference signal oscillator 11, a counting-down circuit 12, a phase comparator (PD) 13, a loop filter (LPF) 14, VCO (VoltageControlled Oscillator: voltage controlled oscillator)15, the comparison counting-down circuit 16, and CPU17 in drawing 3 .
[0004] The above-mentioned counting-down circuit 12, a phase comparator (PD) 13, and the comparison counting-down circuit 16 constitute the PLL circuit 18 as a whole, and CPU17 controls the PLL circuit 18 to output a control signal to each part and to obtain a predetermined synthesizer output. As a reference signal oscillator 11, a crystal oscillator with stability high as a reference frequency f tcxo oscillator is used. If reference frequency f tcxo is inputted from the reference signal oscillator 11, a counting-down circuit 12 will output the reference signal f r (=f tcxo/R) which carried out reference frequency f tcxo of the reference signal oscillator 11 R dividing, and carried out it R dividing to a phase comparator (PD) 13.
[0005] A phase comparator (PD) 13 carries out the phase comparison of comparison signal f r' (=f vco/N) which carried out N dividing of the reference signal f r (=f tcxo/R) carried out R dividing with the counting-down circuit 12, and the signal f vco of VCO15 with the comparison counting-down circuit 16, and outputs the error signal to a loop filter (LPF) 14. A loop filter (LPF) 14 integrates with the inputted error signal, changes it into error voltage, and applies this error voltage to the control terminal of VCO15. VCO15 acquires the signal which operated so that this might become f r=f r', and kept the frequency of f vco=f rxN constant.
[0006] On the other hand, the PLL frequency synthesizer circuit formed into many circuits as shown in drawing 4 is in one of the frequency change improvement in the speed. Drawing 4 is the example of the PLL frequency synthesizer circuit made into two circuits among the formation of many circuits. In drawing 4 , the many circuits-ized PLL frequency synthesizer circuit 20 is constituted by the reference signal oscillator 21, the PLL circuits 22 and 23, VCO 24 and 25, and an output selection switch (SW)26 and CPU27. The above-mentioned PLL circuits 22 and 23 serve as the same circuitry as the PLL circuit 18 shown in drawing 3 .
[0007] The above-mentioned reference signal oscillator 21, the PLL circuit 22, VCO24, and an output selection switch (SW)26 and CPU27 The 1st PLL frequency synthesizer circuit 28 as a whole the reference signal oscillator 21, the PLL circuit 23, VCO25, and an output selection switch (SW)26 and CPU27 [moreover,] The 2nd PLL frequency synthesizer circuit 29 is constituted as a whole. The output

of the 1st PLL frequency synthesizer circuit 28, and the output of the 2nd PLL frequency synthesizer circuit 29 It changes to a high speed with the output selection switch (SW) 26 which received the change control signal from CPU27. The signal which the output of two PLL frequency synthesizer circuits 28 and 29 was changed by this at high speed, and kept the frequency constant on a different frequency can be acquired.

[0008]

[Problem(s) to be Solved by the Invention] However, if it was in such a conventional PLL frequency synthesizer circuit formed into many circuits, by having formed many circuits, interference of the signal by the oscillator circuit of each PLL frequency synthesizer circuit increased, and there was a trouble that spurious (interference noise) one will occur or the consumed electric current will increase. In order to prevent interference of a signal, a cure, such as shielding each oscillator-circuit section etc. or fully preparing spacing of each synthesizer, is needed. Moreover, although there are approaches, such as stopping the current supply to VCO of those who are not using it to increase of the consumed electric current by having formed many circuits, when approaches, such as stopping the current supply to VCO, are taken, there is a fault of taking time amount until it takes the time amount to the oscillation at the time of a reboot or a frequency becomes stable.

[0009] Then, this invention does not have interference of the signal by each oscillator-circuit section, and aims at offering the multi-circuit PLL frequency synthesizer circuit in which a high-speed frequency change is possible with a low power.

[0010]

[Means for Solving the Problem] The PLL frequency synthesizer circuit by this invention for the above-mentioned purpose achievement The phase comparison of the signal which carried out dividing of the reference frequency outputted from the reference signal oscillator and the signal frequency outputted from the voltage controlled oscillator is carried out with a phase comparator. While having two or more circuits of PLL frequency synthesizer circuits which make a phase error an electrical-potential-difference value with a loop filter, are returned to a voltage controlled oscillator and make regularity signal frequency of the output of a voltage controlled oscillator It is the PLL frequency synthesizer circuit equipped with a selection means to choose the output of said two or more-circuit PLL frequency synthesizer circuit. The voltage controlled oscillator of said PLL frequency synthesizer circuit chosen by said selection means possesses the standby circuit which shortens the time amount which this voltage controlled oscillator oscillates at the time of a reboot.

[0011] By charging the capacitor inside said voltage controlled oscillator beforehand, said standby circuit may remove the charging time of this capacitor, and may shorten the time amount to an oscillation at the time of a reboot as indicated by claim 2.

[0012] Said standby circuit may have the mode of operation which makes said voltage controlled oscillator operating state, and the standby mode changed into the standby condition of shortening the time amount which this voltage controlled oscillator oscillates at the time of a reboot as indicated by claim 3.

[0013] Moreover, said standby circuit has the mode of operation which makes said voltage controlled oscillator operating state, and the standby mode changed into the standby condition of shortening the time amount which this voltage controlled oscillator oscillates at the time of a reboot, and it makes this mode of operation and a standby mode correspond to the change of the output frequency of said two or more-circuit PLL frequency synthesizer circuit, and you may make it change it as a desirable mode, as indicated by claim 4.

[0014] Moreover, said standby circuit as indicated by claim 5 It has the mode of operation which makes said voltage controlled oscillator operating state, and the standby mode changed into the standby condition of shortening the time amount which this voltage controlled oscillator oscillates at the time of a reboot. While making the standby circuit of the 1st PLL frequency synthesizer circuit into a mode of operation at the time of use of the 1st PLL frequency synthesizer circuit and making a voltage controlled oscillator into operating state The standby circuit of the 2nd PLL frequency synthesizer circuit is made into a standby mode, and you may make it suspend the oscillation of a voltage controlled oscillator.

[0015]
[Function] In this invention, a PLL frequency synthesizer circuit is equipped with two or more circuits, is constituted, and is alternatively changed in the output of a two or more-circuit PLL frequency synthesizer circuit. Furthermore, the standby circuit which shortens the time amount which a voltage controlled oscillator oscillates at the time of a reboot is prepared. In this condition, according to a steady state, at the time of use of the 1st PLL frequency synthesizer circuit, the standby circuit of the 1st PLL frequency synthesizer circuit is made into a mode of operation, a voltage controlled oscillator will be in operating state, the standby circuit of the 2nd PLL frequency synthesizer circuit is made into a standby mode, and the oscillation of a voltage controlled oscillator stops. Moreover, in the time of the change of a frequency, it is made to correspond to the change of the output frequency of a two or more-circuit PLL frequency synthesizer circuit, and a mode of operation and a standby mode are changed.
[0016] Therefore, there is no interference of the signal by each oscillator-circuit section, and a low power can realize the multi-circuit PLL frequency synthesizer circuit in which a high-speed frequency change is possible.
[0017]
[Example] Hereafter, the example of this invention is explained with reference to a drawing. Drawing 1 and drawing 2 are drawings showing one example of the PLL frequency synthesizer circuit concerning this invention, and this example is an example applied to the 2 circuit PLL frequency synthesizer circuit. First, a configuration is explained. Drawing 1 is the block diagram of a 2 circuit PLL frequency synthesizer circuit. drawing 1 -- setting -- the 2 circuit PLL frequency synthesizer circuit 30 -- the reference signal oscillator 31, the PLL circuits (PLL frequency synthesizer circuit) 32 and 33, and a loop filter 1 (LPF1) -- 34, 35, and a loop filter 2 (LPF2) -- it is constituted by 36, 37, VCO (voltage controlled oscillator) 38 and 39, the standby circuits (STBY) 40 and 41, and an output selection switch (SW)42 and CPU43.
[0018] moreover, the above-mentioned PLL circuits 32 and 33 -- counting-down circuits 44 and 45 and a phase comparator (PD) -- it is constituted by 46, 47, electronic switches (change means) 48 and 49, and the comparison counting-down circuits 50 and 51. As a reference signal oscillator 31, a crystal oscillator with stability high as a reference frequency f tcxo oscillator is used.
[0019] counting-down circuits 44 and 45 -- the reference frequency f tcxo of the reference signal oscillator 31 -- R -- the reference signal f r (=f tcxo/R) which carried out dividing and which was carried out R dividing -- a phase comparator (PD) -- it outputs to 46 and 47. Phase comparator (PD) 46 and 47 carry out the phase comparison of comparison signal f r' (=f vco/N) which carried out N dividing of the signal f vco of the reference signals 38 and VCO [fr (=f tcxo/R) and] 39 carried out R dividing with counting-down circuits 44 and 45 with the comparison counting-down circuits 50 and 51, and output the error signal to electronic switches 48 and 49. the comparison counting-down circuits 50 and 51 -- the output signal f vco from VCO 38 and 39 -- N dividing -- carrying out -- as comparison signal f r' (=f vco/N) -- a phase comparator (PD) -- it is made to return to 46 and 47 The frequency of a synthesizer is selected by changing this division ratio N. electronic switches 48 and 49 -- the error signal from the comparison counting-down circuits 50 and 51 -- the loop filter 1 (LPF1) for spurious removal -- 34, 35, or a loop filter 2 (LPF2) -- it changes and outputs to 36 and 37.
[0020] a loop filter 1 (LPF1) -- 34 and 35 -- the original loop filter 2 (LPF2) -- independently [36 and 37], it is the filter prepared in spurious removal, and the time constant of a filter is set up for a long time, and spurious generating by interference is prevented. however -- since a response characteristic falls -- electronic switches 48 and 49 -- a loop filter 1 (LPF1) -- 34, 35, or a loop filter 2 (LPF2) -- it is used, changing 36 and 37. a loop filter 2 (LPF2) -- 36 and 37 consist of low pass filters -- having -- a phase comparator (PD) -- it integrates with the error signal from 46 and 47, a high-frequency component is removed, it changes into error voltage, and this error voltage is applied to the control terminal of VCO 38 and 39.
[0021] VCO 38 and 39 -- a loop filter 2 (LPF2) -- the signalling frequency which operated so that it might become f r=f r' with the error voltage from 36 and 37, and kept the frequency of f vco=f r/N constant is outputted. The standby circuits (STBY) 40 and 41 are circuits which make possible high-

speed starting of VCO 38 and 39, and are controlled by the control signal from CPU27. It mentions later by drawing 2 .

[0022] The output selection switch (SW) 42 can acquire the signal which changed the output of VCO 38 and 39 to the high speed with the change control signal from CPU27, and kept the frequency constant on a different frequency. CPU43 controls the PLL circuits 32 and 33, the standby circuits (STBY) 40 and 41, and the output selection switch (SW) 42 to output a control signal to each part and to obtain a predetermined synthesizer output.

[0023] The above-mentioned reference signal oscillator 31, the PLL circuit 32, loop filter 1 (LPF1) 34, loop filter 2 (LPF2) 36, VCO38, the standby circuit (STBY) 40, and an output selection switch (SW)42 and CPU43 The 1st PLL frequency synthesizer circuit 52 is constituted as a whole. Again The reference signal oscillator 31, the PLL circuit 33, loop filter 1 (LPF1) 35, loop filter 2 (LPF2) 37, VCO39, the standby circuit (STBY) 41, and an output selection switch (SW)42 and CPU43 The 2nd PLL frequency synthesizer circuit 53 is constituted as a whole.

[0024] Drawing 2 is drawing for explaining the function of the above-mentioned standby circuits (STBY) 40 and 41. As mentioned above, there were approaches, such as stopping the current supply to VCO of those who are not using it to increase of the consumed electric current by having formed many circuits, but when this approach was taken, there was a fault of taking time amount until it takes the time amount to the oscillation at the time of a reboot or a frequency becomes stable. The capacitor for noise rejection exists in the interior of VCO, and after current supply stopping to VCO, that reason needs to charge this capacitor, when oscillating at the time of a reboot. Therefore, the time amount to the oscillation at the time of a reboot will be taken for the charging time of a capacitor.

[0025] Then, high-speed starting of VCO 38 and 39 is made possible by forming the standby circuits (STBY) 40 and 41 which charge beforehand the capacitor for noise rejection of the above VCO 38 and the 39 interior, and controlling the standby circuits (STBY) 40 and 41 by this example with the control signal from CPU27. In this case, the standby circuits (STBY) 40 and 41 have the mode of operation which makes VCO 38 and 39 operating state, and the standby mode changed into the standby condition of shortening the time amount which VCO 38 and 39 oscillates at the time of a reboot, make these modes of operation and a standby mode correspond to the change of the output frequency of the PLL frequency synthesizer circuits 52 and 53, and change it.

[0026] Next, an operation is explained. The 2 circuit PLL frequency synthesizer circuit 30 of this example repeats (1) steady state described below and the condition at the time of (2) frequency change, and operates.

(1) As for VCO38, steady state one PLL frequency synthesizer circuit (for example, 1st PLL frequency synthesizer circuit 52) is operating by the standby circuit (STBY) 40 of the 1st PLL frequency synthesizer circuit 52 serving as a mode of operation at the time of actuation, the output of VCO38 is locked by predetermined frequency by the PLL circuit 32, and the output selection switch (SW) 42 is operating so that the signalling frequency from VCO38 may be outputted.

[0027] If the condition that PLL has started is explained concretely, the reference signal f r (=f tcxo/R) with which the counting-down circuit 44 carried out reference frequency f tcxo of the reference signal oscillator 31 R dividing, and carried out it R dividing will be outputted to a phase comparator (PD) 46. A phase comparator (PD) 46 carries out the phase comparison of comparison signal f r' (=f vco/N) which carried out N dividing of the reference signal f r (=f tcxo/R) carried out R dividing with the counting-down circuit 44, and the signal f vco of VCO38 with the comparison counting-down circuit 50, and outputs the error signal to loop filter 2 (LPF2) 36. Loop filter 2 (LPF2) 36 integrate with the inputted error signal, change it into error voltage, and apply this error voltage to the control terminal of VCO38. VCO38 acquires the signal which operated so that this might become f r=f r', and kept the frequency of f vco=f rxN constant.

[0028] Then, the standby circuit (STBY) 41 of the PLL frequency synthesizer circuit (in this case, 2nd PLL frequency synthesizer circuit 53) of another side serves as a standby mode, and VCO39 is in a standby condition. Since VCO39 is in a standby condition, the oscillation based on VCO39 does not take place, and it does not generate spurious one by interference of the signal by each oscillator-circuit

section.
[0029] (2) Set the value of the counter according to the frequency changed to PLL actuation of the PLL frequency synthesizer circuit (in this case, 2nd PLL frequency synthesizer circuit 53) which is in a standby condition at the time of a frequency change. Moreover, VCO39 of a standby condition considers as operating state, and VCO38 of operating state is changed into a standby condition, and changes the output selection switch (SW) 42. It operates so that may start VCO39 at high speed since the capacitor for the noise rejection of the VCO39 interior is beforehand charged by the standby circuit (STBY) 41 prepared in VCO39 at this time, and loop filter 1 (LPF1) 35 may be further changed to loop filter 2 (LPF2) 37 by the electronic switch 49 the early stages of a response, the time constant of a loop filter may be lowered and an oscillation frequency may be doubled with a high speed. Although it becomes easy to generate spurious one by lowering the time constant of a loop filter in early stages of a response, it ignores about spurious generating and a response characteristic is thought as important the early stages of a response.
[0030] As mentioned above, although the actuation which performs a frequency change was shown from the steady state from which it is the 1st PLL frequency synthesizer circuit 52 at the time of operation, and the standby circuit (STBY) 41 of the 2nd PLL frequency synthesizer circuit 53 ** serves as a standby mode, it is also completely the same as when reverse.
[0031] Thus, in this example, it sets in the 2 circuit PLL frequency synthesizer circuit 30. To VCO38 of the 1st PLL frequency synthesizer circuit 52, and VCO39 of the 2nd PLL frequency synthesizer circuit 53 Form the standby circuits (STBY) 40 and 41, respectively, for example, make the standby circuit (STBY) 40 into a mode of operation at the time of PLL frequency synthesizer circuit 52 use, and only VCO38 is made into operating state. Spurious generating according the oscillation of VCO39 to interference of a stop and a signal is prevented by making the standby circuit (STBY) 41 of the PLL frequency synthesizer circuit 53 of another side into a standby mode, and changing VCO39 into a standby condition. Moreover, at the time of a frequency change, by the standby circuits (STBY) 40 and 41, VCO39 of a standby condition is made into operating state, and VCO38 of operating state is changed into a standby condition. By this, VCO39 can be started at high speed and a high-speed frequency change can be realized.
[0032] furthermore, the electronic switches 48 and 49 -- the loop filter 1 (LPF1) for spurious removal -- 34, 35, and a loop filter 2 (LPF2) -- spurious generating prevention and coexistence of a response characteristic can be aimed at by using it, changing 36 and 37.
[0033] In addition, although it is the example applied to the 2 circuit PLL frequency synthesizer circuit as a many circuits-ized PLL frequency synthesizer circuit in this example, as long as a PLL frequency synthesizer circuit is formed into many circuits, the thing of what kind of configuration may be used, and it cannot be overemphasized that what kind of thing is sufficient as the class and the number of each part material, the control approach, etc.
[0034]
[Effect of the Invention] According to this invention, in the multi-circuit PLL frequency synthesizer circuit aiming at a high-speed frequency change, there is no spurious generating by interference of the signal of each oscillation section, the consumed electric currents can also be reduced and abolition of each shielding or simplification, and high-density-assembly-ization are attained. Moreover, the increments in the consumed electric current by the formation of many circuits can also be few, and many circuits-ization can be positively performed now.

[Translation done.]